

1. A method with trench source to increase the coupling of source to floating gate comprising the steps of:

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providing a substrate having a source region;

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forming a split-gate flash memory cell on said substrate;

forming a trench source in said source region;

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performing a source implant;

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forming a gate oxide layer over the inside walls of said trench source;

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performing a lateral diffusion of said source implant; and

performing thermal cycle of said substrate.

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2. The method of claim 1, wherein said substrate is silicon.

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3. The method of claim 1, wherein said trench source has tilted walls.

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4. The method of claim 3, wherein said tilted walls have an included angle between about 10 to 45 degrees.

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5. The method of claim 1, wherein said source implant comprises phosphorous (P) ions at a dosage level between about 1×10^{15} to 1×10^{16} atoms/cm² and energy between about 10 to 50 KeV.

6. The method of claim 1, wherein said source implant is performed at a tilt angle between about 10 to 45 degrees.

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7. The method of claim 1, wherein said gate oxide layer has a thickness between about 4 to 70 Å.

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8. The method of claim 1, wherein said lateral diffusion of said source implant is accomplished at a temperature between about 850 to 950 °C.

9. The method of claim 1, wherein said thermal cycle is performed between temperatures about 850 to 950 °C.

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10. A method with trench source to increase the coupling of source to floating gate comprising the steps of:

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providing a substrate having active and passive regions

defined;

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forming a first gate oxide layer over said substrate;

9 forming a first polysilicon layer over said gate oxide
layer;

12 forming a nitride layer over said first polysilicon layer;

patterning said nitride layer to expose a portion of said
15 first polysilicon layer to define a floating gate area;

performing oxidation of said portion of said first
18 polysilicon layer to form a polyoxide layer over said first
polysilicon layer;

21 etching said first polysilicon layer using said polyoxide
layer as a hard mask to form a floating gate;

24 forming an interpoly oxide over said polyoxide;

forming a second polysilicon layer over said interpoly
27 oxide;

patterning said second polysilicon layer to form a control

30 gate;

forming a trench source in said substrate;

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performing a source implant;

36 forming a second gate oxide layer over the inside walls of
said trench source;

39 performing a lateral diffusion of said source implant; and

performing thermal cycle of said substrate.

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11. The method of claim 10, wherein said substrate is
silicon.

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12. The method of claim 10, wherein said forming said first
gate oxide layer is accomplished by thermal growth at a
3 temperature between about 800 to 950 °C.

13. The method of claim 10, wherein said first gate oxide
layer has a thickness between about 70 to 90 angstroms (Å).

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14. The method of claim 10, wherein said forming said
first polysilicon layer is accomplished with silicon source

3 SiH₄ using LPCVD at a temperature between about 530 to 650 °C.

15. The method of claim 10, wherein said first polysilicon layer has a thickness between about 900 to 1100 Å.

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16. The method of claim 10, wherein said forming said nitride layer over said first polysilicon layer is accomplished by CVD at a temperature between about 650 to 800°C by reacting dichlorosilane (SiCl₂H₂) with ammonia (NH₃).

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17. The method of claim 10, wherein the thickness of said nitride layer is between about 700 to 900 Å.

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18. The method of claim 10, wherein said oxidation of said first polysilicon layer to form poly-oxide is accomplished through thermal oxidation at a temperature between about 800 to 950 °C.

19. The method of claim 10, wherein said polyoxide layer has a thickness between about 1100 to 1300 Å.

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20. The method of claim 10, wherein said interpoly oxide comprises a layer of first thermal oxide, a layer of high

3 temperature oxide (HTO), and a layer of second thermal oxide.

21. The method of claim 20, wherein said first thermal oxide layer has a thickness between about 30 to 50 Å, and is
3 thermally grown at a temperature between about 800 to 950 °C.

22. The method of claim 20, wherein said HTO layer has a thickness between about 120 to 140 Å, and is deposited at a
3 temperature between about 800 to 950 °C.

23. The method of claim 20, wherein said second thermal oxide layer has a thickness between about 60 to 80 Å, and is
3 thermally grown at a temperature between about 800 to 950 °C.

24. The method of claim 10, wherein said forming said second polysilicon layer is accomplished with silicon source
3 SiH₄ using LPCVD at a temperature between about 530 to 650 °C.

25. The method of claim 10, wherein said second polysilicon layer has a thickness between about 1900 to 2100
3 Å.

26. The method of claim 10, wherein said trench source has a depth between about 200 to 600 Å.

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27. The method of claim 10, wherein said trench source has tilted walls.

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28. The method of claim 27, wherein said tilted walls have an included angle between about 10 to 45 degrees.

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29. The method of claim 10, wherein said source implant comprises phosphorous (P) ions at a dosage level between about 1×10^{15} to 1×10^{16} atoms/cm² and energy between about 10 to 50 KeV.

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30. The method of claim 10, wherein said source implant is performed at a tilt angle between about 10 to 45 degrees.

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31. The method of claim 10, wherein said second gate oxide layer is thermally grown at a temperature between about 800 to 950 °C.

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32. The method of claim 10, wherein said second gate oxide layer has thickness between about 60 to 80 Å.

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33. The method of claim 10, wherein said lateral diffusion of said source implant is accomplished at a temperature between about 800 to 950 °C.

34. The method of claim 10, wherein said thermal cycle is performed between temperatures about 800 to 950 °C.

35. A split-gate flash memory cell having a trench source with tilted walls comprising:

a substrate having a source region;

a split-gate flash memory cell on said substrate;

a trench source in said source region;

a gate oxide layer over the inside walls of said trench source; and

a laterally enlarged diffused area of said source region.

36. The split-gate flash memory cell of claim 35, wherein said trench has a depth between about 200 to 600 Å.

37. The split-gate flash memory cell of claim 35, wherein said trench has tilted walls.

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38. The split-gate flash memory cell of claim 35, wherein said tilted walls have an included angle between about 10 to 45 degrees.

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39. The split-gate flash memory cell of claim 35, wherein said trench source is implanted at a tilt angle between about 10 to 45 degrees.

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40. The split-gate flash memory cell of claim 35, wherein said gate oxide layer has a thickness between about 60 to 80 Å.

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41. The split-gate flash memory cell of claim 35, wherein said laterally enlarged diffused area spans at least one-half the width of said floating gate.

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